Amendments to the Specification

Please replace the title at page 1, lines 1 through 2 with the following amended title:

~~DELAYED~~ DELAY LOCKED LOOP IMPLEMENTATION IN A SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

Please replace the paragraph at page 5, lines 21 through 31 with the following amended paragraph:

In accordance with an embodiment of the invention, a clock applying circuit for a synchronous memory is comprised of a clock input for receiving a clock input signal, apparatus connected to the synchronous memory for receiving a driving clock signal, and a tapped delay line for receiving the clock input signal and for delivering the ~~clock~~ driving clock signal to the synchronous memory in synchronism with but delayed ~~fro~~ from the clock input signal, the delay being a small fraction of the clock period of the clock input signal. The fraction can be negligibly small.

Please replace the paragraph at page 8, line 32 through page 9, line 2 with the following amended paragraph:

The delay locked loop can be disabled and the regular buffered version of the system clock can be used as in the prior art, enabling the output buffer with the prior art form of delayed clock signal, which can allow the system to be tested or operated using a low frequency clock.